The main goal of sub- or near-threshold design (i.e. integrated circuits supplied with a voltage lower or just above MOS transistor threshold voltage) is to reduce the dynamic power consumption by decreasing the supply voltage. Working at lower voltages than regular circuits opens the door to better power efficiency. However, at these low voltages, digital standard cell libraries need to be revisited to ensure the correct operation of integrated circuits. To fulfill the requirements of the specific application, libraries can also be optimized for constraints like frequency or static power consumption. This motivates the comprehensive study of trade-offs in the design of sub- and near-threshold standard cell libraries. A first library for the EM Microelectronic Marin ALP 180 nm technology has been developed focusing on ultra-low-power optimization by limiting the leakage power within given frequency requirements. A second library for TSMC 65 nm has been developed to reach the minimum supply voltage level for applications with energy harvesting. Both libraries will be used as building blocks for the circuit integrations planned in the icySoC project in order to demonstrate the capabilities of sub- and near-threshold design.

**Building blocks for low-power circuits**

- Early specification and careful selection and development of the building blocks of low-power circuits (e.g. standard cell libraries) ensure successful design for a given application (i.e. dynamic power, static power and frequency requirements)
- **ROM Memories**
- **SRAM Memories (next step in the project)**
- **And others…**

**ALP 180 nm standard cell library**

- **Libraries considered**
  - SUB_LIB_SVT: standard-V\(^{TH}\) library sized for 0.6 V min.
  - SUB_LIB_LVT: low-V\(^{TH}\) library sized for 0.4 V min.
  - LIB_SVT: standard-V\(^{TH}\) library from the foundry at 0.9 V min.
  - LIB_LVT: low-V\(^{TH}\) library from the foundry at 0.72 V min.

**Test vehicle circuit evaluation**

- Test vehicle: digital circuit using latch-based design with a critical path depth of 45 cells and an equivalent gate count of 10’000 gates

**TSMC 65 nm standard cell library**

- **Libraries considered**
  - SUB_LIB_LVT: low-V\(^{TH}\) library sized for 0.3 V min.
  - LIB_HVT: high-V\(^{TH}\) library from the foundry operating at 1.0 V min.

**Test vehicle circuit evaluation**

- Test vehicle: CSEM’s icyflex2 ultra-low-power processor in battery operated applications, such as portable medical and wireless sensors. It can also be used as an microcontroller core, in a larger SoC, e.g. for handling power management.

**Sub- & near-threshold standard cell choices**

- **V\(^{TH}\) selection**
  - low-V\(^{TH}\) \(\rightarrow\) lower minimum V\(^{DD}\)
  - high-V\(^{TH}\) \(\rightarrow\) lower leakage

- **Minimum V\(^{DD}\) selection**
  - low-V\(^{DD}\) \(\rightarrow\) enables energy harvesting
  - high-V\(^{DD}\) \(\rightarrow\) lower upsize of W and L for robust operation

- **W/L selection**
  - Inverse Narrow Width Effect \(\rightarrow\) W upsize causes V\(^{TH}\) increase
  - Reverse Short Channel Effect \(\rightarrow\) L upsize causes V\(^{TH}\) decrease

**Results in Tables I and II are normalized to the LIB_HVT flip-flop icyflex2 implementation.**

**Table I: Comparison of the TSMC 65 nm libraries for flip-flop based design**

<table>
<thead>
<tr>
<th>Application</th>
<th>V(^{DD})</th>
<th>Power/Frequency</th>
<th>Area</th>
<th>Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>LIB_HVT 1.0V</td>
<td>1.03 E-1</td>
<td>2.12</td>
<td>4.60 E-1</td>
<td>2.12</td>
</tr>
<tr>
<td>SUB_LIB_LVT 0.3V</td>
<td>1.55 E-2</td>
<td>2.12</td>
<td>4.60 E-1</td>
<td>2.12</td>
</tr>
<tr>
<td>SUB_LIB_LVT 0.5V</td>
<td>1.55 E-2</td>
<td>2.12</td>
<td>4.60 E-1</td>
<td>2.12</td>
</tr>
</tbody>
</table>

**Table II: Comparison of the TSMC 65 nm libraries for latch based design**

<table>
<thead>
<tr>
<th>Application</th>
<th>V(^{DD})</th>
<th>Power/Frequency</th>
<th>Area</th>
<th>Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>LIB_HVT 1.0V</td>
<td>1.80 E-4</td>
<td>3.80 E-2</td>
<td>1.04</td>
<td>2.10</td>
</tr>
<tr>
<td>SUB_LIB_LVT 0.3V</td>
<td>2.60 E-5</td>
<td>1.15 E-2</td>
<td>1.04</td>
<td>2.10</td>
</tr>
<tr>
<td>SUB_LIB_LVT 0.5V</td>
<td>2.60 E-5</td>
<td>1.15 E-2</td>
<td>1.04</td>
<td>2.10</td>
</tr>
</tbody>
</table>

**Table III: Comparison of considered ALP018 libraries (normalized values)**

**ALP 180 nm library selected**

- SUB_LIB_SVT: standard-V\(^{TH}\), V\(^{DD}\)=0.54 V min, L=300 nm, 72 cells
- Goal: Frequency at 0.9 V similar to LIB_LVT at 0.72 V and static power at 0.6 V comparable to LIB_SVT at 0.9 V
- Works in a wide range of power supplies

**ALP 180 nm library selected**

- SUB_LIB_LVT: low-V\(^{TH}\), V\(^{DD}\)=0.3 V min, L=100 nm, 50 cells
- Goal: min V\(^{DD}\) for enabling energy harvesting
- Works in a wide range of power supplies
- Interest of latch based design for sub- and near-threshold operation