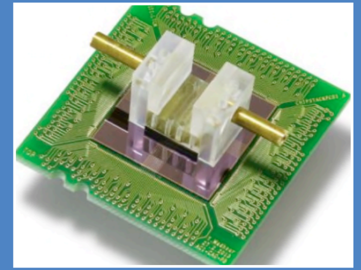
Prof. John Thome, EPFL

CMOSAIC

3D STACKED ARCHITECTURES WITH INTERLAYER COOLING



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What it's about…

Designing multi-layered computer chips with interlayer cooling for increased computing performance and reduced energy consumption

Context and project goals

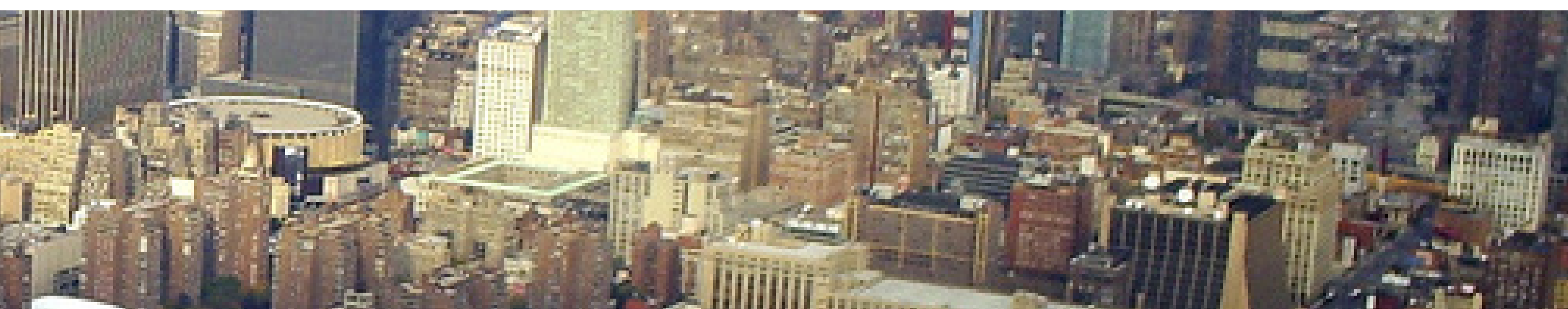
The project addresses interlayer cooling of 3D computer chips, including water cooling, two-phase refrigerant cooling, development and perfection of new micro-fabrication techniques for TSVs and their connections, bonding of stacked layers together, dynamic thermal modeling of 3D chips, and extensive experimental testing of 2D and 3D cooling solutions and new thermal models.

How the project differentiates from similar competition in the field

Other labs are not as advanced in the thermal modeling of the underlying heat transfer processes nor in the manufacturing and testing of 3D test vehicles.

Quick summary of the project status and key results

CMOSAIC has combined the most advanced microscale heat transfer experiments and modeling with the most advanced 3D manufacturing developments, thus building the most convincing 3D test vehicles to date on the 3D-IC roadmap for development of the next generation of high performance computing within 3D architectures the size of a sugar cube cooled with microchannels. The teamwork has produced final 3D test vehicles which have four-thousand TSV's inside connected to numerous local heaters and resistance thermometers. The packaging of this 3D vehicle not only allows the flow of electricity through the device but also the flow of coolant though all its layers for the removal of large heat densities. This is combined with the development of the most advanced 3D thermal simulation codes now available for both single-phase cooling and two-phase cooling, including both very fast simulators for rapid analysis and a very detailed simulator with the first ever combined heat and two-phase flow spreading capabilities.



Success stories

Awards

Outstanding Paper Award, ICEPT HDP 2012 Conference (International Conference on Electronic Packaging Technology and High Density Packaging) for the following paper: Madhour, Y., Brunschwiler, T., El Kazzi, M., Thome, J.R., Michel, B., "Patterned die-to-die thin film bonding for 3D chip stacks with integrated microfluidic cooling", International Conference on Electronic Packaging Technology and High Density Packaging, 2012. The award ceremony took place at this year's ICEPT-HDP 2013 conference. The prize was awarded for a concept for a scalable integrated cooling technique that requires a novel die-to-die solder bonding method. The bonding method they designed and successfully tested exploits patterned thin-film lead-free solder and meets the challenges posed by integrating state-of-the-art cooling structures into a 3D chip stack, such as minimizing the gap between the dies, sealing the active solder pads from a conductive coolant fluid, and sealing the edges of the chip to prevent leakage.

Production of the final CMOSAIC package demonstrating packaging and cooling technologies for future interlayer cooled 3D chip stacks:

The package consists of five 380μm-thick 12.7x12.7 mm2 silicon chips flip-chip bonded to form the chip stack. These chips represent mock-ups of real devices, with controlled resistive heaters acting as processor cores and embedded microchannels on the back for integrated cooling. The reason why the consortium considers the packaging/interlayer cooling technologies developed in CMOSAIC as a success story is because they demonstrate the feasibility at an early stage of industrial development. The availability of such demonstrators helps to accelerate the development of the industry towards this new direction.

Main publications

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